FIG. 1

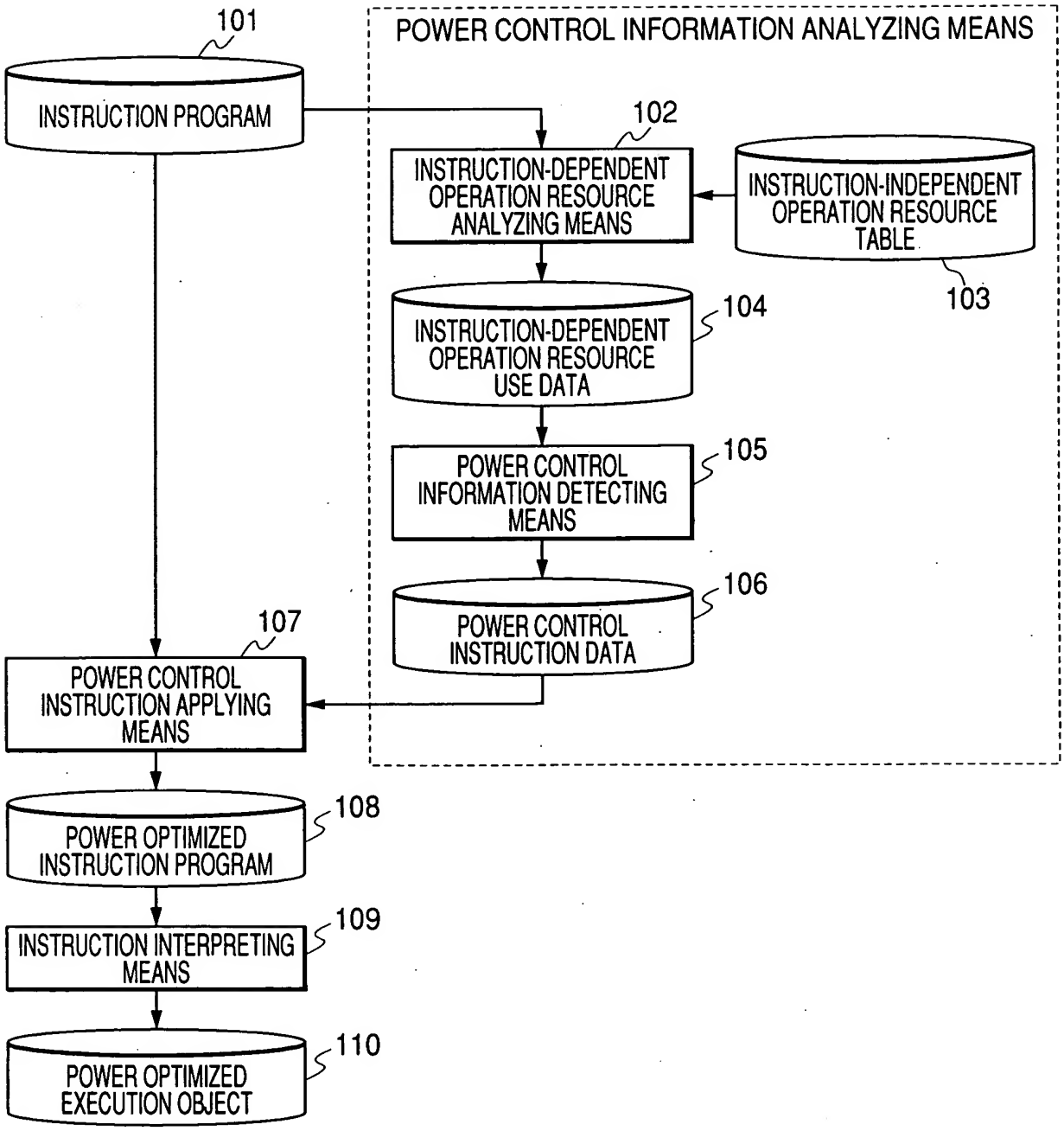
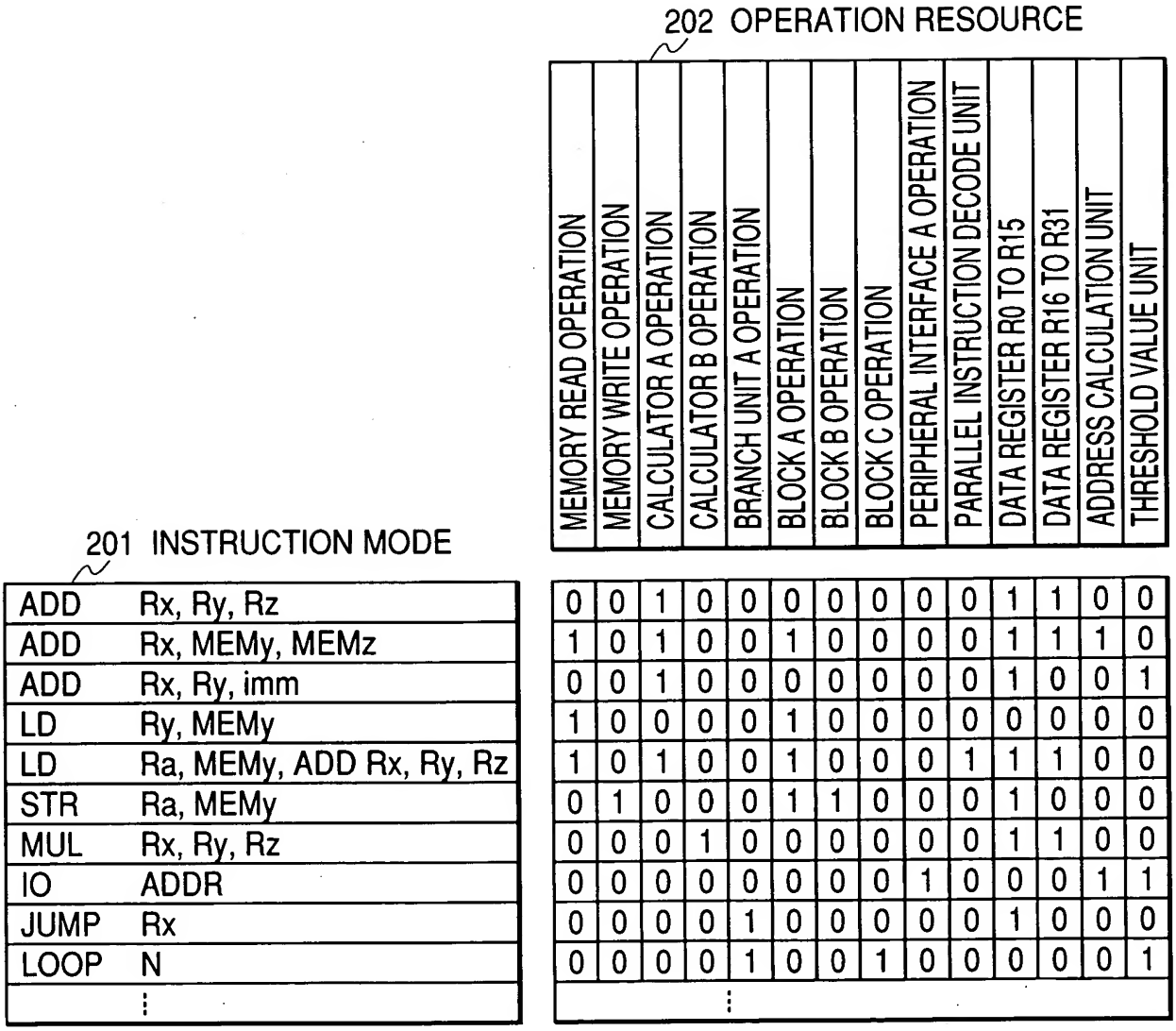


FIG. 2



INSTRUCTION-INDEPENDENT OPERATION RESOURCE TABLE

FIG. 3

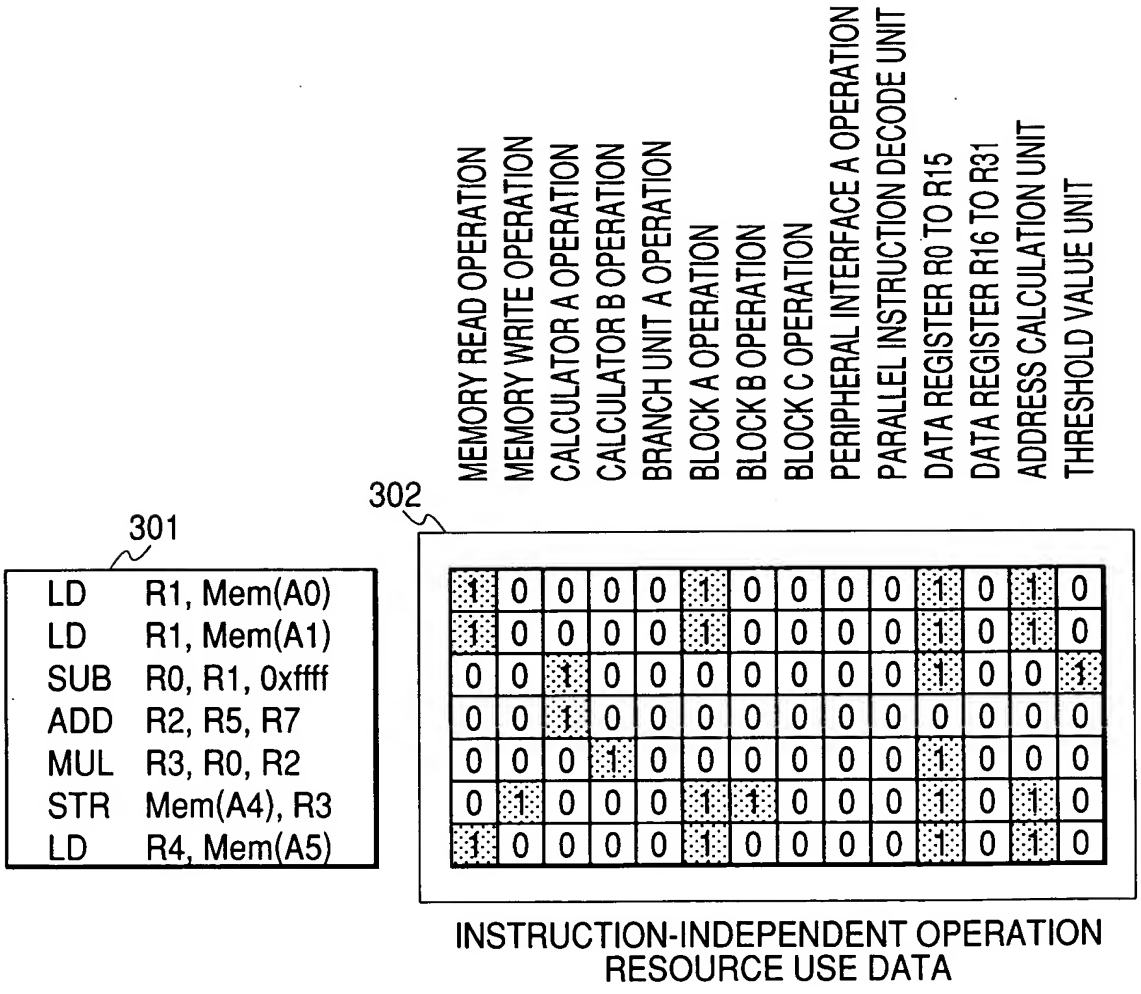

301
LD R1, Mem(A0)
LD R1, Mem(A1)
SUB R0, R1, 0xffff
ADD R2, R5, R7
MUL R3, R0, R2
STR Mem(A4), R3
LD R4, Mem(A5)
302
MEMORY READ OPERATION
MEMORY WRITE OPERATION
CALCULATOR A OPERATION
CALCULATOR B OPERATION
BRANCH UNIT A OPERATION
BLOCK A OPERATION
BLOCK B OPERATION
BLOCK C OPERATION
PERIPHERAL INTERFACE A OPERATION
PARALLEL INSTRUCTION DECODE UNIT
DATA REGISTER R0 TO R15
DATA REGISTER R16 TO R31
ADDRESS CALCULATION UNIT
THRESHOLD VALUE UNIT
1 0 0 0 0 1 0 0 0 0 1 0 1 0
1 0 0 0 0 1 0 0 0 0 1 0 1 0
0 0 1 0 0 0 0 0 0 0 1 0 0 1
0 0 1 0 0 0 0 0 0 0 0 0 0 0
0 0 0 1 0 0 0 0 0 0 1 0 0 0
0 1 0 0 0 1 1 0 0 0 1 0 1 0
1 0 0 0 0 1 0 0 0 0 1 0 1 0
INSTRUCTION-INDEPENDENT OPERATION RESOURCE USE DATA

FIG. 4

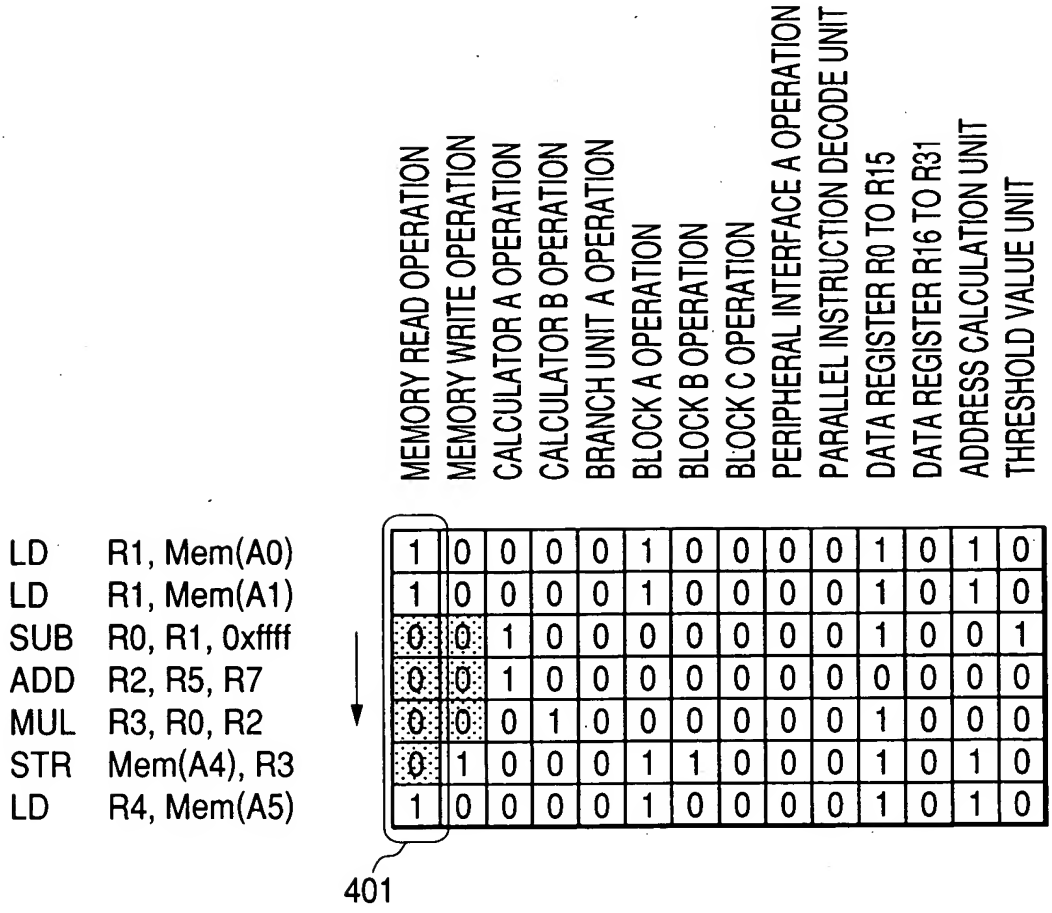

MEMORY READ OPERATION
MEMORY WRITE OPERATION
CALCULATOR A OPERATION
CALCULATOR B OPERATION
BRANCH UNIT A OPERATION
BLOCK A OPERATION
BLOCK B OPERATION
BLOCK C OPERATION
PERIPHERAL INTERFACE A OPERATION
PARALLEL INSTRUCTION DECODE UNIT
DATA REGISTER R0 TO R15
DATA REGISTER R16 TO R31
ADDRESS CALCULATION UNIT
THRESHOLD VALUE UNIT
LD R1, Mem(A0)
LD R1, Mem(A1)
SUB R0, R1, 0xffff
ADD R2, R5, R7
MUL R3, R0, R2
STR Mem(A4), R3
LD R4, Mem(A5)
1 0 0 0 0 1 0 0 0 0 1 0 1 0
1 0 0 0 0 1 0 0 0 0 1 0 1 0
0 0 1 0 0 0 0 0 0 0 1 0 0 1
0 0 1 0 0 0 0 0 0 0 0 0 0 0
0 0 0 1 0 0 0 0 0 0 1 0 0 0
0 1 0 0 0 1 1 0 0 0 1 0 1 0
1 0 0 0 0 1 0 0 0 0 1 0 1 0
401

FIG. 5

```
LD          R1, Mem(A0)
LD          R1, Mem(A1)
SET PCR     #Memory_Read_Stop
SUB         R0, R1, 0xffff
ADD         R2, R5, R7
MUL         R3, R0, R2
STR         Mem(A4), R3
CLR PCR     #Memory_Read_Stop
LD          R4, Mem(A5)
```

FIG. 6

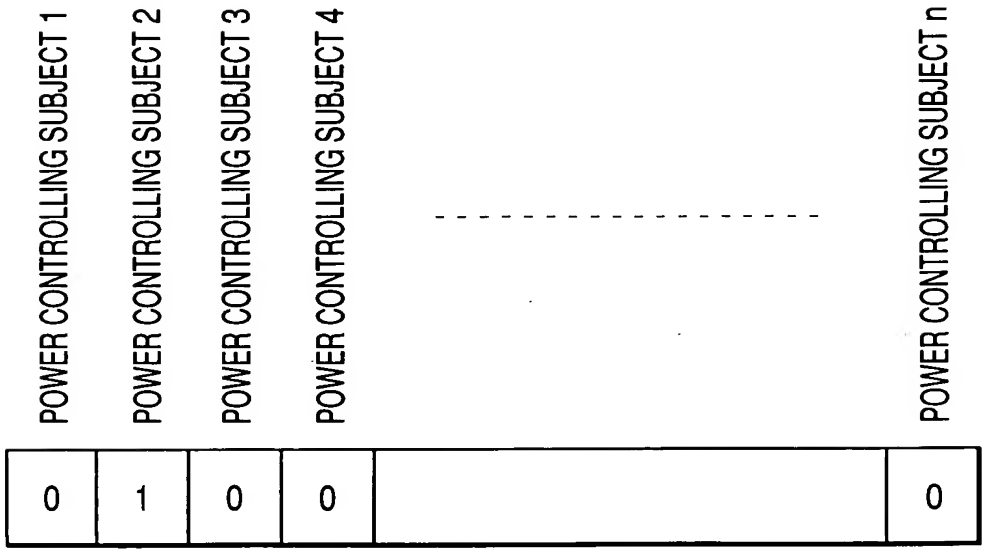


FIG. 7

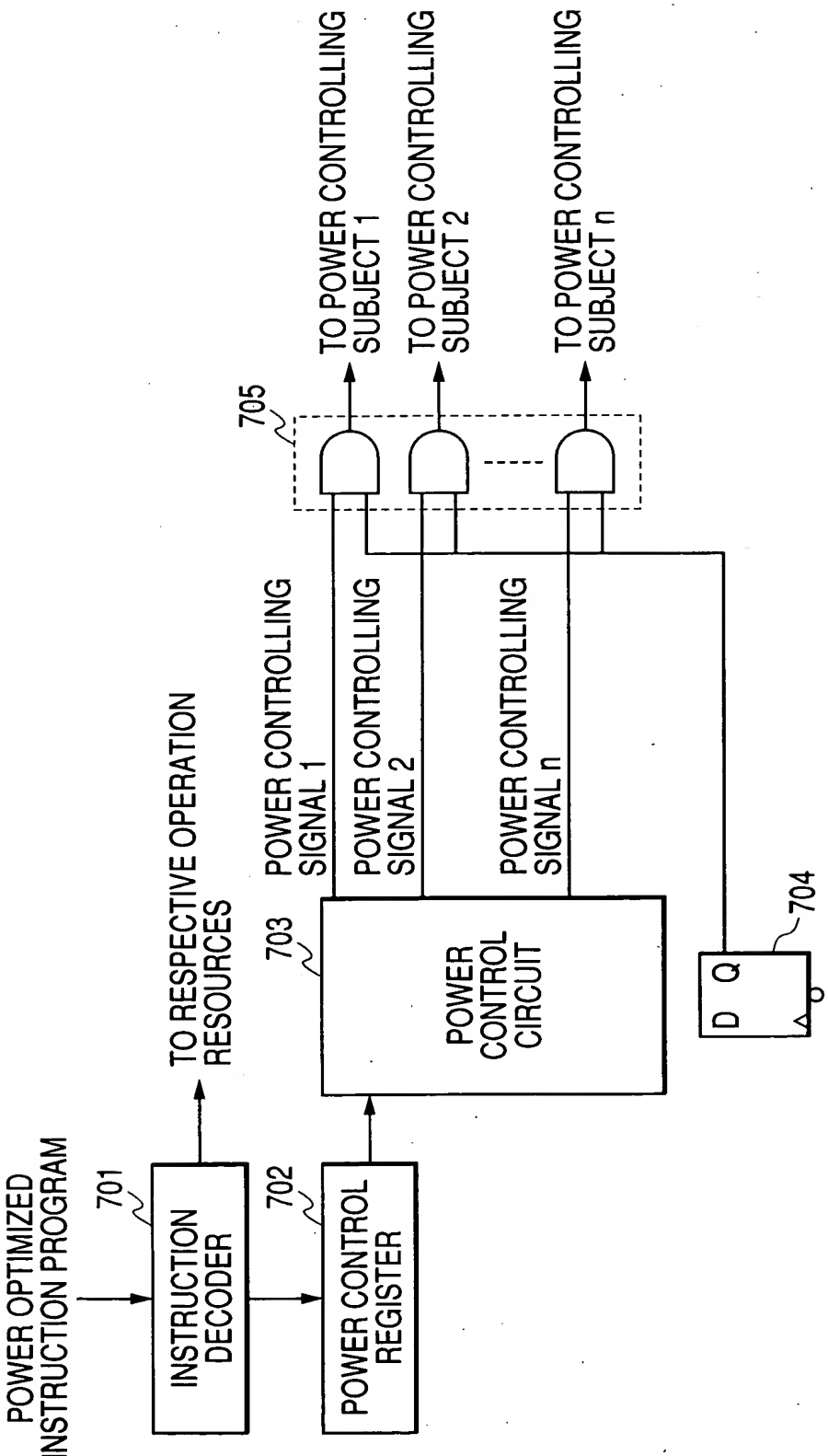

POWER OPTIMIZED INSTRUCTION PROGRAM
701
INSTRUCTION DECODER
702
POWER CONTROL REGISTER
TO RESPECTIVE OPERATION RESOURCES
703
POWER CONTROL CIRCUIT
POWER CONTROLLING SIGNAL 1
POWER CONTROLLING SIGNAL 2
POWER CONTROLLING SIGNAL n
705
TO POWER CONTROLLING SUBJECT 1
TO POWER CONTROLLING SUBJECT 2
TO POWER CONTROLLING SUBJECT n
704
D Q

FIG. 8

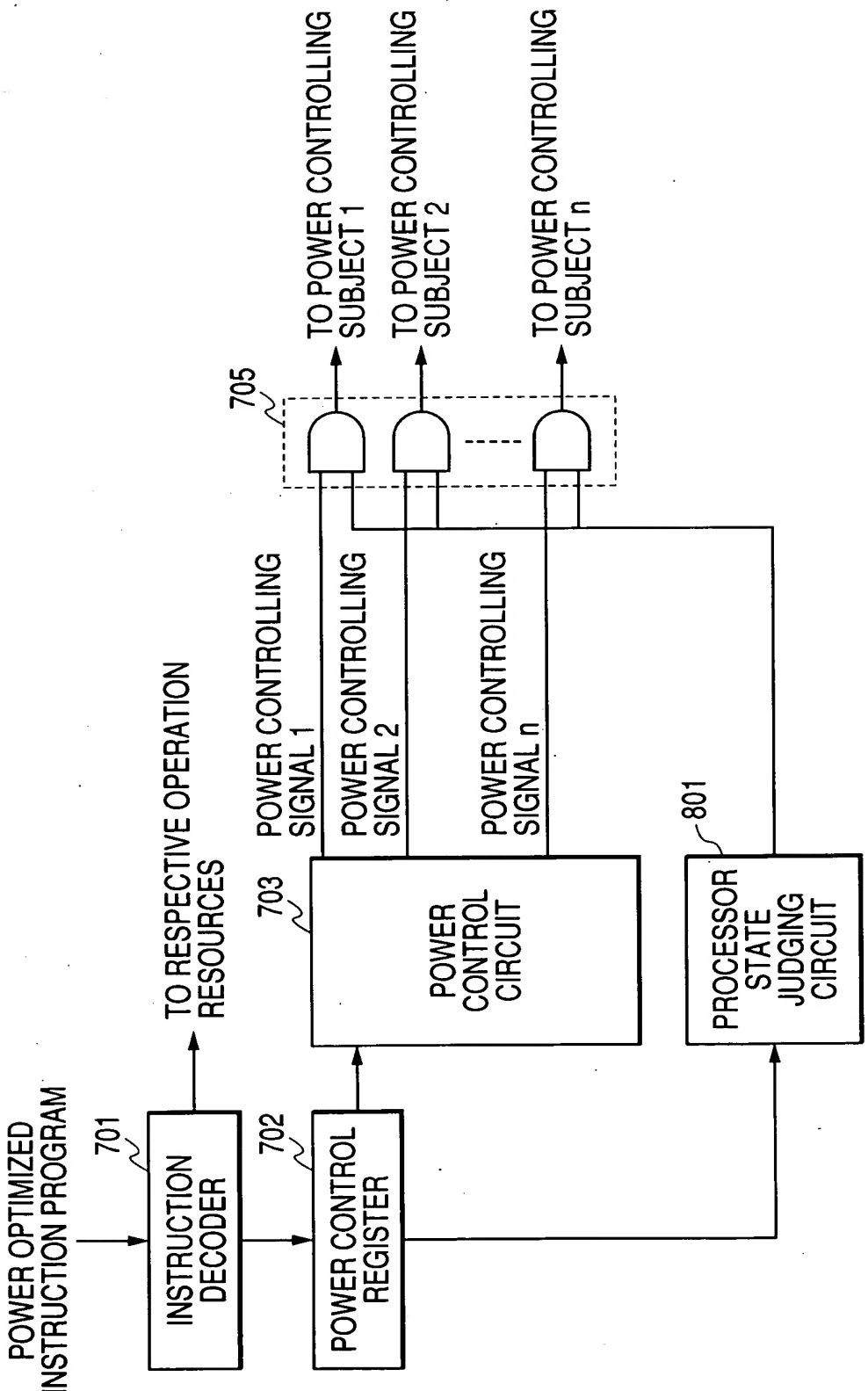

POWER OPTIMIZED INSTRUCTION PROGRAM
701
INSTRUCTION DECODER
TO RESPECTIVE OPERATION RESOURCES
702
POWER CONTROL REGISTER
703
POWER CONTROL CIRCUIT
POWER CONTROLLING SIGNAL 1
POWER CONTROLLING SIGNAL 2
POWER CONTROLLING SIGNAL n
705
TO POWER CONTROLLING SUBJECT 1
TO POWER CONTROLLING SUBJECT 2
TO POWER CONTROLLING SUBJECT n
801
PROCESSOR STATE JUDGING CIRCUIT

FIG. 9

PROGRAM ID	POWER CONTROL FUNCTION ON/OFF
ID1	ON
ID2	ON
ID3	OFF
ID4	ON

FIG. 10

```
data_a = data_b*1.75;
data_c = func_calc_d(in1, in2, in3);

if(cond_k==1) {adrs1 = adrs1+8;}

#pragma POWER_CONT_ON_Level1
for(i=0; i<256; i++) {
  out_sum = out_sum*data_c[adrs1]
}
#pragma POWER_CONT_OFF

if(out_sum>24) {adrs1 = adrs1+32;}
```

FIG. 11

LEVEL	CONTROL CONTENT
LEVEL 0	ONLY OPERATION RESOURCE WHICH CAN BE STOPPED IS DETECTED BY REPLACING INSTRUCTIONS
LEVEL 1	OPERATION RESOURCE WHICH IS NOT ACTUATED FOR 10, OR MORE SECTIONS IS DETECTED
LEVEL 2	OPERATION RESOURCE WHICH IS NOT ACTUATED FOR 5, OR MORE SECTIONS IS DETECTED
LEVEL 3	OPERATION RESOURCE WHICH IS NOT ACTUATED FOR 3, OR MORE SECTIONS IS DETECTED

FIG. 12

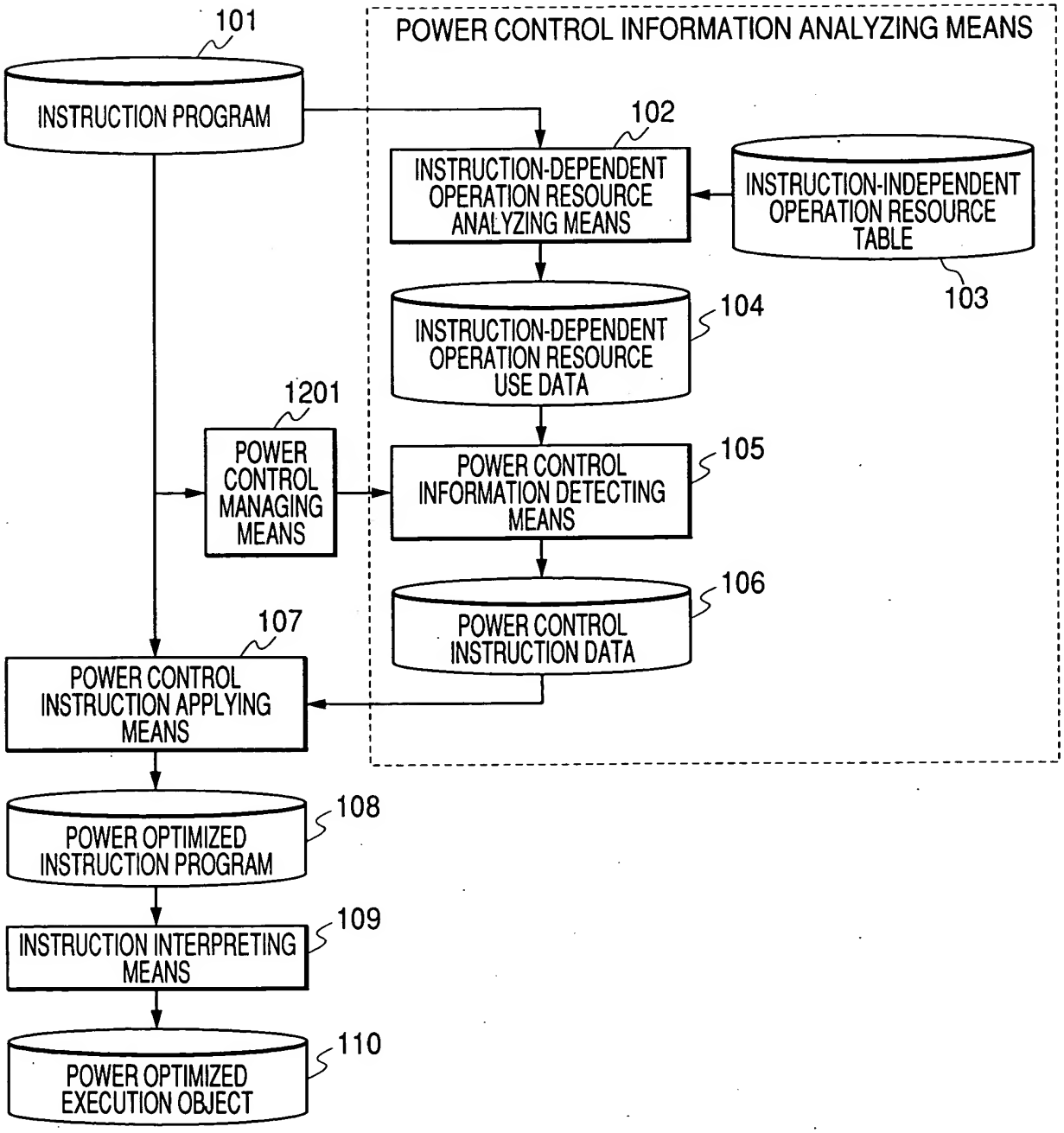

101
INSTRUCTION PROGRAM
POWER CONTROL INFORMATION ANALYZING MEANS
102
INSTRUCTION-DEPENDENT OPERATION RESOURCE ANALYZING MEANS
INSTRUCTION-INDEPENDENT OPERATION RESOURCE TABLE
103
INSTRUCTION-DEPENDENT OPERATION RESOURCE USE DATA
104
1201
POWER CONTROL MANAGING MEANS
POWER CONTROL INFORMATION DETECTING MEANS
105
POWER CONTROL INSTRUCTION DATA
106
107
POWER CONTROL INSTRUCTION APPLYING MEANS
POWER OPTIMIZED INSTRUCTION PROGRAM
108
INSTRUCTION INTERPRETING MEANS
109
POWER OPTIMIZED EXECUTION OBJECT
110

FIG. 13

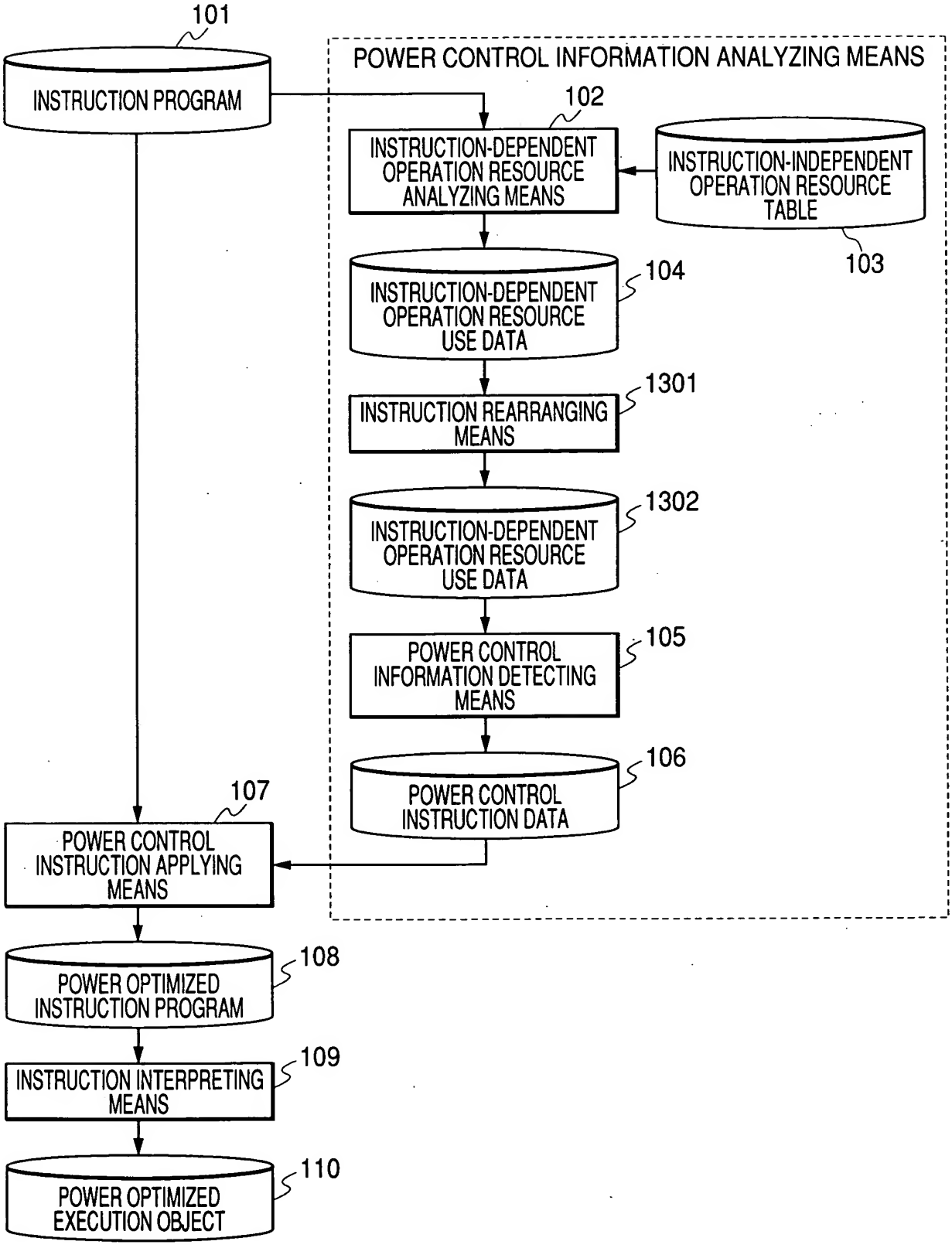

101
INSTRUCTION PROGRAM
POWER CONTROL INFORMATION ANALYZING MEANS
102
INSTRUCTION-DEPENDENT OPERATION RESOURCE ANALYZING MEANS
INSTRUCTION-INDEPENDENT OPERATION RESOURCE TABLE
103
INSTRUCTION-DEPENDENT OPERATION RESOURCE USE DATA
104
INSTRUCTION REARRANGING MEANS
1301
INSTRUCTION-DEPENDENT OPERATION RESOURCE USE DATA
1302
POWER CONTROL INFORMATION DETECTING MEANS
105
POWER CONTROL INSTRUCTION DATA
106
107
POWER CONTROL INSTRUCTION APPLYING MEANS
POWER OPTIMIZED INSTRUCTION PROGRAM
108
INSTRUCTION INTERPRETING MEANS
109
POWER OPTIMIZED EXECUTION OBJECT
110

FIG. 14

		MEMORY READ OPERATION	MEMORY WRITE OPERATION	CALCULATOR A OPERATION	CALCULATOR B OPERATION	BRANCH UNIT A OPERATION	BLOCK A OPERATION	BLOCK B OPERATION	BLOCK C OPERATION	PERIPHERAL INTERFACE A OPERATION	PARALLEL INSTRUCTION DECODE UNIT	DATA REGISTER R0 TO R15	DATA REGISTER R16 TO R31	ADDRESS CALCULATION UNIT	THRESHOLD VALUE UNIT
MOV	R0, 0X00aa	0	0	1	0	0	0	0	0	0	0	1	0	0	1
ADD	R5, R5, R0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
LD	R1, Mem(A1)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
SUB	R0, R1, 0X0fff	0	0	1	0	0	0	0	0	0	0	1	0	0	1
LD	R7, Mem(A0)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
ADD	R2, R5, R7	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MUL	R3, R0, R2	0	0	0	1	0	0	0	0	0	0	1	0	0	0
STR	Mem(A4), R3	0	1	0	0	0	1	1	0	0	0	1	0	1	0

FIG. 15

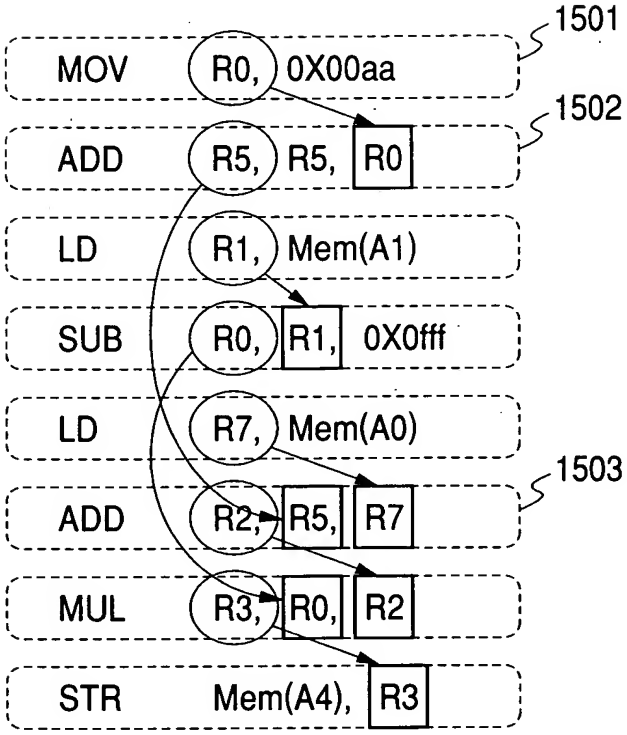

1501
MOV R0, 0X00aa
1502
ADD R5, R5, R0
LD R1, Mem(A1)
SUB R0, R1, 0X0fff
LD R7, Mem(A0)
1503
ADD R2, R5, R7
MUL R3, R0, R2
STR Mem(A4), R3

FIG. 16

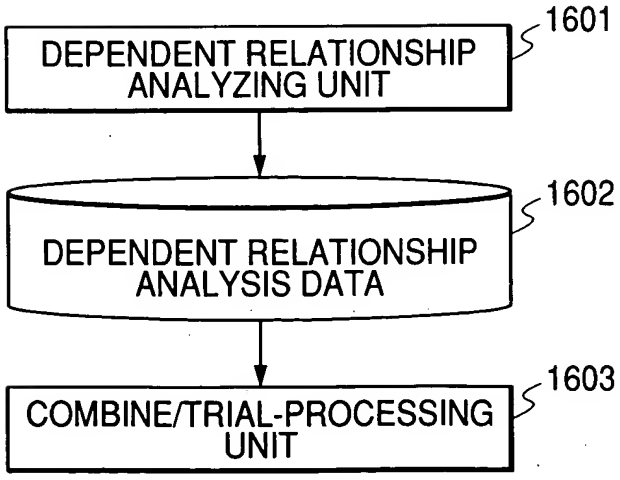

1601
DEPENDENT RELATIONSHIP ANALYZING UNIT
1602
DEPENDENT RELATIONSHIP ANALYSIS DATA
1603
COMBINE/TRIAL-PROCESSING UNIT

FIG. 17

		MEMORY READ OPERATION	MEMORY WRITE OPERATION	CALCULATOR A OPERATION	CALCULATOR B OPERATION	BRANCH UNIT A OPERATION	BLOCK A OPERATION	BLOCK B OPERATION	BLOCK C OPERATION	PERIPHERAL INTERFACE A OPERATION	PARALLEL INSTRUCTION DECODE UNIT	DATA REGISTER R0 TO R15	DATA REGISTER R16 TO R31	ADDRESS CALCULATION UNIT	THRESHOLD VALUE UNIT
LD	R1, Mem(A1)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
LD	R7, Mem(A0)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
MOV	R0, 0X00aa	0	0	1	0	0	0	0	0	0	0	1	0	0	1
ADD	R5, R5, R0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
SUB	R0, R1, 0X0fff	0	0	1	0	0	0	0	0	0	0	1	0	0	1
ADD	R2, R5, R7	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MUL	R3, R0, R2	0	0	0	1	0	0	0	0	0	0	1	0	0	0
STR	Mem(A4), R3	0	1	0	0	0	1	1	0	0	0	1	0	1	0

FIG. 18

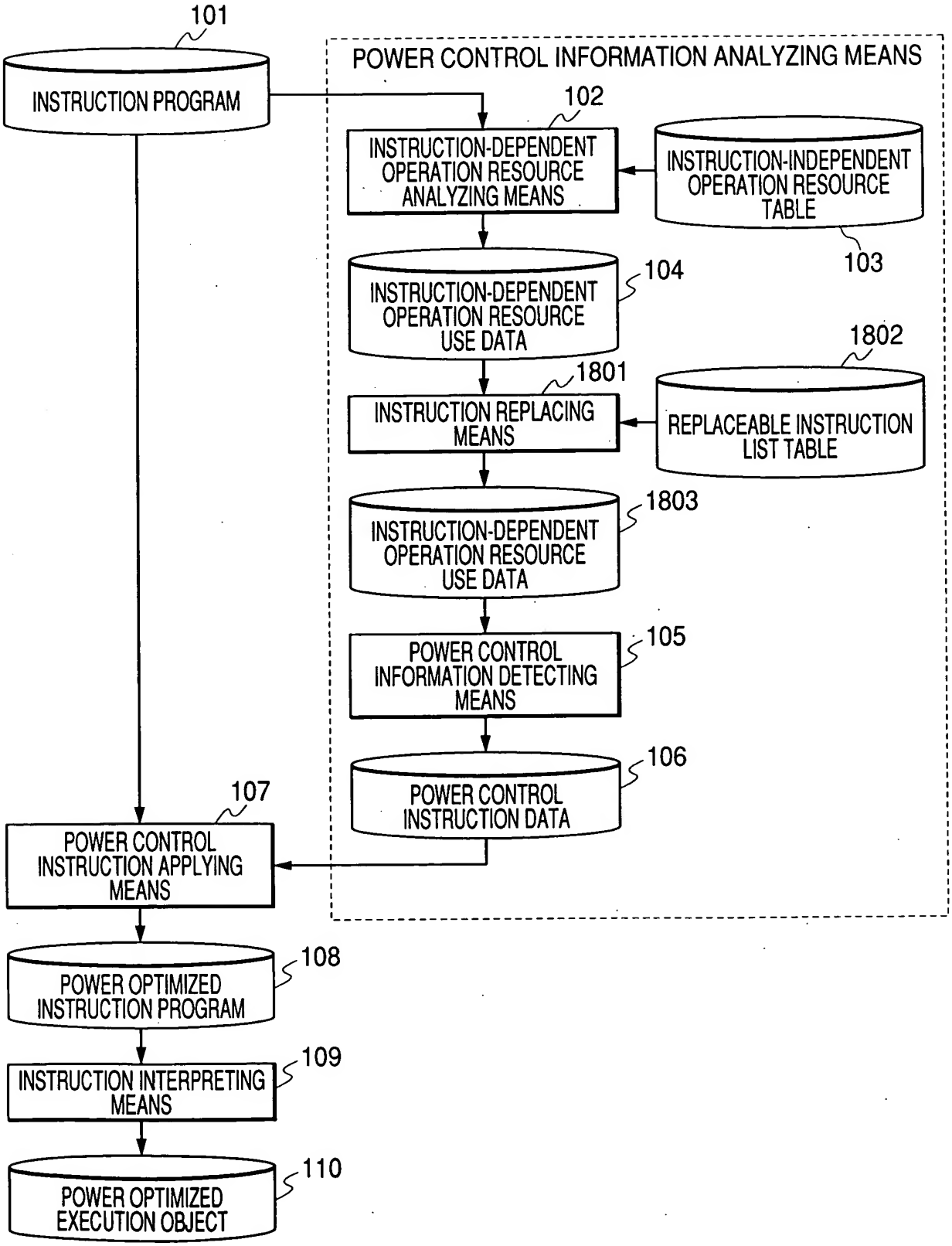

101
INSTRUCTION PROGRAM
POWER CONTROL INFORMATION ANALYZING MEANS
102
INSTRUCTION-DEPENDENT OPERATION RESOURCE ANALYZING MEANS
INSTRUCTION-INDEPENDENT OPERATION RESOURCE TABLE
103
INSTRUCTION-DEPENDENT OPERATION RESOURCE USE DATA
104
1802
1801
INSTRUCTION REPLACING MEANS
REPLACEABLE INSTRUCTION LIST TABLE
INSTRUCTION-DEPENDENT OPERATION RESOURCE USE DATA
1803
POWER CONTROL INFORMATION DETECTING MEANS
105
POWER CONTROL INSTRUCTION DATA
106
107
POWER CONTROL INSTRUCTION APPLYING MEANS
POWER OPTIMIZED INSTRUCTION PROGRAM
108
INSTRUCTION INTERPRETING MEANS
109
POWER OPTIMIZED EXECUTION OBJECT
110

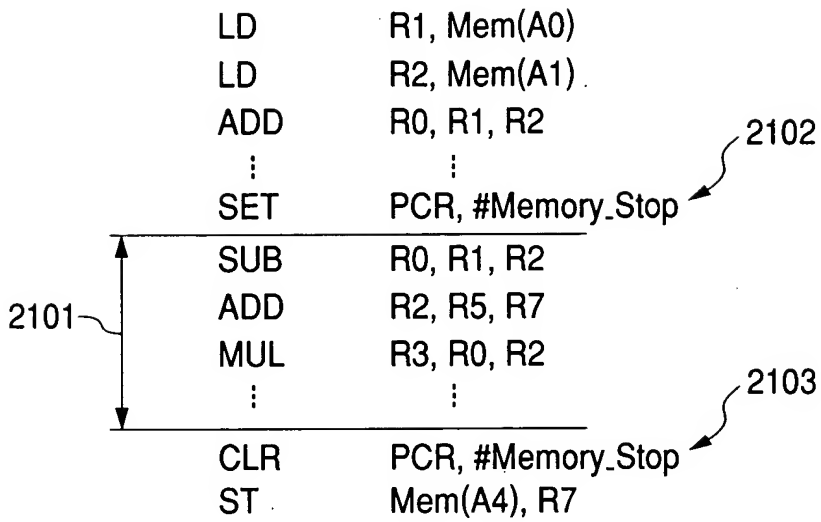
FIG. 19

		MEMORY READ OPERATION	MEMORY WRITE OPERATION	SHIFTER OPERATION	MULTIPLIER OPERATION	BRANCH UNIT A OPERATION	BLOCK A OPERATION	BLOCK B OPERATION	BLOCK C OPERATION	PERIPHERAL INTERFACE A OPERATION	PARALLEL INSTRUCTION DECODE UNIT	DATA REGISTER R0 TO R15	DATA REGISTER R16 TO R31	ADDRESS CALCULATION UNIT	THRESHOLD VALUE UNIT
STR	Mem(A2), R9	0	0	1	0	0	0	0	0	0	0	1	0	0	1
MUL	R3, R0, 0x0002	0	0	0	1	0	0	0	0	0	0	1	0	0	0
LD	R1, Mem(A1)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
MUL	R5, R7, 0x0004	0	0	0	1	0	0	0	0	0	0	1	0	0	0
SUB	R0, R1, 0x0fff	0	0	1	0	0	0	0	0	0	0	1	0	0	0
ADD	R2, R5, R7	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MUL	R3, R0, R2	0	0	0	1	0	0	0	0	0	0	1	0	0	0
STR	Mem(A4), R3	0	1	0	0	0	1	1	0	0	0	1	0	1	0

FIG. 20

		MEMORY READ OPERATION	MEMORY WRITE OPERATION	SHIFTER OPERATION	MULTIPLIER OPERATION	BRANCH UNIT A OPERATION	BLOCK A OPERATION	BLOCK B OPERATION	BLOCK C OPERATION	PERIPHERAL INTERFACE A OPERATION	PARALLEL INSTRUCTION DECODE UNIT	DATA REGISTER R0 TO R15	DATA REGISTER R16 TO R31	ADDRESS CALCULATION UNIT	THRESHOLD VALUE UNIT
STR	Mem(A2), R9	0	0	1	0	0	0	0	0	0	0	1	0	0	1
SFT	R3, R0, 0x0001	0	0	1	0	0	0	0	0	0	0	1	0	0	0
LD	R1, Mem(A1)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
SFT	R5, R7, 0x0002	0	0	1	0	0	0	0	0	0	0	1	0	0	0
SUB	R0, R1, 0x0fff	0	0	1	0	0	0	0	0	0	0	1	0	0	0
ADD	R2, R5, R7	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MUL	R3, R0, R2	0	0	0	1	0	0	0	0	0	0	1	0	0	0
STR	Mem(A4), R3	0	1	0	0	0	1	1	0	0	0	1	0	1	0

FIG. 21


LD R1, Mem(A0)
LD R2, Mem(A1)
ADD R0, R1, R2
SET PCR, #Memory_Stop
SUB R0, R1, R2
ADD R2, R5, R7
MUL R3, R0, R2
CLR PCR, #Memory_Stop
ST Mem(A4), R7
2101
2102
2103